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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,322	07/01/2003	Manoj Kumar	52669_CIP1	4030

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,322	KUMAR ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/1/*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13, 16-20, 22, 25-29, 31, 34-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Wert et al (5,406,140).

Claim 13, Wert shows an electronic circuit (118, Fig. 3) comprising:

an input logic inverter (350, 354) operating at a first voltage level (EXTVDD) and having an input and an output, the input for receiving an input signal at the first voltage level;

an output logic inverter (386, 390) operating at a second voltage level (VDDI) lower than the first voltage level and having an input and an output for providing an output signal (Y) of the electronic circuit; and

voltage reduction means (358, 382, 378) connected between the output of said input logic inverter and the input of said output logic inverter;

the input logic inverter, said output logic inverter, and said voltage reduction means cooperating to reduce the input signal from the first voltage level to the second voltage level provide the output signal so that the input and output signals have substantially equal rise and fall delays and substantially equal rise and fall transition times.

Claim 16, Wert shows voltage reduction means reduces a voltage level of the input signal to between a first threshold below the first voltage level and a second threshold above the first voltage level (the threshold voltage of transistor 358).

Claims 17, Wert shows output logic inverter comprises at least one output transistor (390), and wherein the second threshold corresponds an upper voltage limit for the at least one output transistor.

Claim 18, Wert shows the output logic inverter comprises at least one output transistor (390), and wherein the first threshold corresponds to a threshold voltage of said at least one output transistor.

Claim 19, Wert shows further first logic circuit (114) operating at the first voltage level and providing the input signal to the input of said input logic inverter; and a second logic circuit (inherent limitation, e.g. internal logic or logic core) operating at the second voltage level for receiving the output signal from output of said output logic inverter.

Claim 20, Wert shows the voltage reduction means provides an output signal (374) that follows an output signal of said input logic inverter until reaching the second voltage second voltage level while the input logic inverter remains above the second voltage level.

The limitations of claims 22, 25-29, 31, and 34-36 are rejected as above claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13-15, 22-24, and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al (4,926,070).

Claim 13, Tanaka shows an electronic circuit (Fig. 4) comprising:

an input logic inverter (41) operating at a first voltage level (VCC) and having an input and an output, the input for receiving an input signal at the first voltage level;

an output logic inverter (46-47) operating at a second voltage level (VPP) higher than the first voltage level and having an input and an output for providing an output signal (Y) of the electronic circuit; and

voltage level shifting means (52) connected between the output of said input logic inverter and the input of said output logic inverter;

the input logic inverter, said output logic inverter, and said voltage means cooperating to reduce the input signal from the first voltage level to the second voltage level provide the output signal so that the input and output signals have substantially equal rise and fall delays and substantially equal rise and fall transition times.

Therefore, Tanaka shows the claimed invention except for the second voltage level lower than the first voltage level. It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement an input circuit with the second voltage level lower than the first voltage level, since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art.

Claim 14, Tanaka shows the voltage reduction means comprises a plurality of series-connected transistors (42, 43) each biased provide a fixed voltage drop.

Claim 15, Tanaka shows the voltage reduction means further comprises a feedback transistor (45) connected between the output and input of the output logic inverter to reduce output leakage current therefrom.

The limitations of claims 22-24 and 31-33 are rejected as above claims.

5. Claims 13, 20-21, 22, 29-30, 31, 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nunogmami (5,136,191).

Claim 13, Nunogmami shows an electronic circuit (Fig. 3) comprising:

an input logic inverter (10) operating at a first voltage level (VDD1) and having an input and an output, the input for receiving an input signal at the first voltage level;

an output logic inverter (14) operating at a second voltage level (VDD2) higher than the first voltage level and having an input and an output for providing an output signal (19) of the electronic circuit; and

voltage level shifting means (28, 29) connected between the output of said input logic inverter and the input of said output logic inverter;

the input logic inverter, said output logic inverter, and said voltage means cooperating to reduce the input signal from the first voltage level to the second voltage level provide the output signal so that the input and output signals have substantially equal rise and fall delays and substantially equal rise and fall transition times.

Therefore, Nunogmami shows the claimed invention except for the second voltage level lower than the first voltage level. It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement an input circuit with the second voltage level lower than the first voltage level, since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art.

Claim 20, Nunogmami shows the voltage reduction means provides an output signal that follows an output signal of said input logic inverter until reaching the second voltage second voltage level while the input logic inverter remains above the second voltage level.

Claim 21, Nunogmami shows the voltage reduction means comprises; a first transistor (29) having a first conduction terminal connected (through transistors 32 & 34) to the second voltage level, a second conduction terminal connected to the input of said output logic inverter, and a control terminal connected to the output of the input logic inverter; and

a second transistor (28)having a first conduction terminal for receiving the input signal, a second conduction terminal connected to the input of said output logic inverter, and a control terminal connected to the output of said input logic inverter.

The limitations of claims 22, 29-30, 31, 36-37 are rejected as above claims.

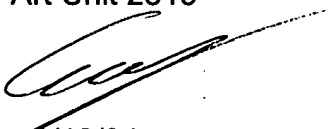
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh Q. Tran
Examiner
Art Unit 2819



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